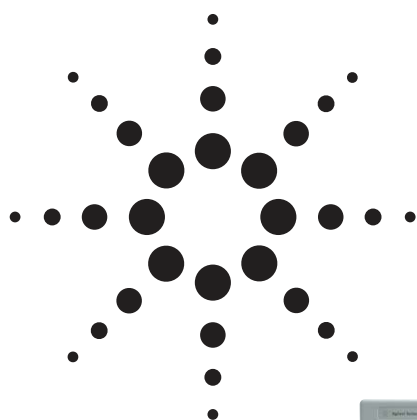# Agilent 81140A Series
81141A / 81142A
Serial Pulse Data Generators
7 GHz and 13.5 GHz

Data Sheet

The smart way to measure – Quality Stimulus Solution Delivering the confidence you demand for your signal integrity in the next speed class

Version 1.1

Key Benefits

- Pulse, Data Pattern and PRBS generation up to 7 GHz and 13.5 GHz
- Differential outputs for data, clock and trigger
- Trigger and external clock input
- Fastest transition times < 20 ps
- Data formats: NRZ, R1 and RZ
- Low jitter, high accuracy signals with Jitter < 1 ps RMS
- 1 GHz jitter modulation bandwidth
- PRBS generation from 2^5–1 to 2^{31}–1
- 32 Mbit Memory for long, "real world" patterns
- Sequencing and looping for protocol based data
- Event trigger capabilities
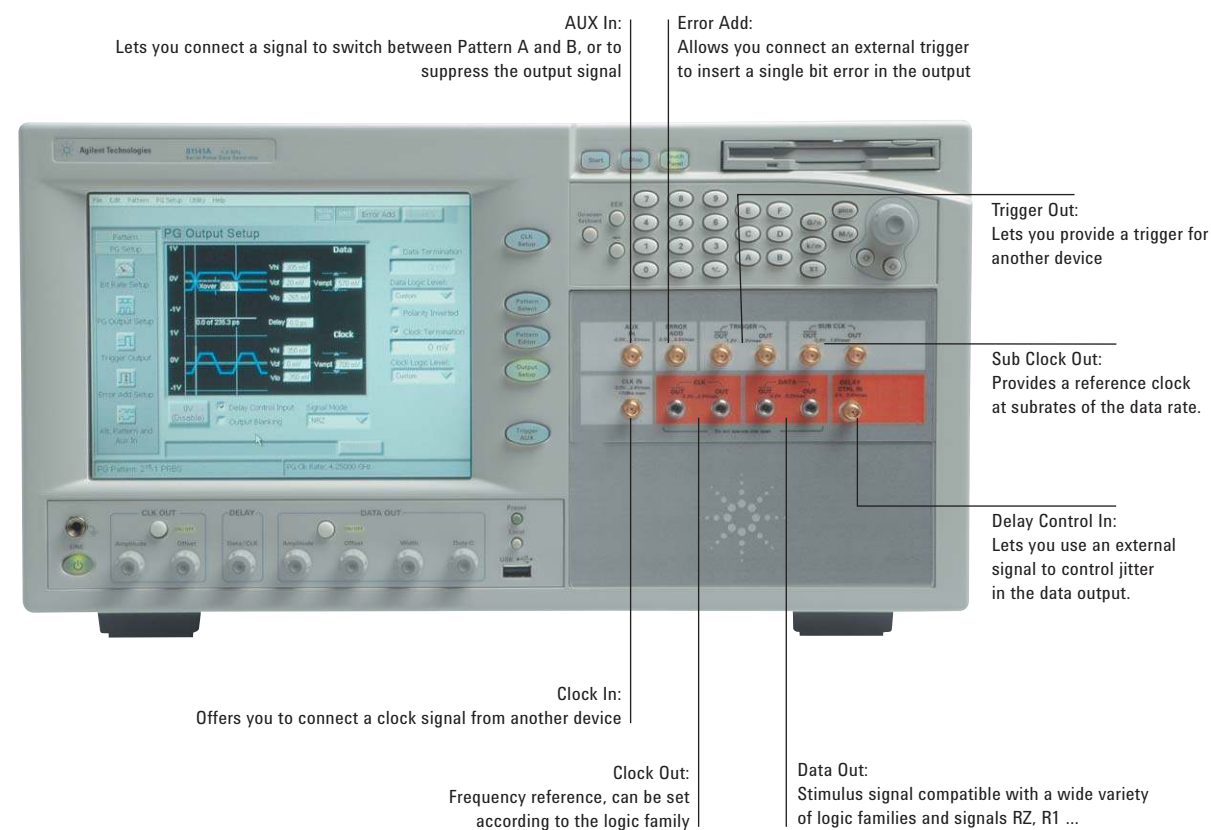- Subrate clock for easy generation of reference clock

Agilent Technologies

81140A Series Serial Pulse Data Generator at a glance

All timing parameters are measured at ECL levels.

Table 1: 81140A series specifications at a glance.

Frequency	150 MHz to 7 GHz / 13.5 GHz
Output channels	Single channel data and clock, differential or single ended
Triggering	Aux In (Trigger In) and Trigger Out
Data formats	RZ, R1, NRZ
Duty cycle	70ps to period −70ps 35ps to period -35ps (Pulse for 81142A only)
Clock/data delay range	±0.75 ns with a 100 fs resolution
Delay modulation range	−100 ps to 100 ps
Transition times (10/90)	< 25 ps
Jitter (clock mode)	1 ps rms typical
Jitter (data mode)	9 ps $_{pp}$ typical
Jitter modulation bandwidth	DC - 1 GHz
Data output amplitude/resolution	0.1 V to 1.8 V with 5 mV resolution
Output voltage window	−2 V to 3 V
Sequencing and looping	1 level of up to 4 blocks
Memory	32 Mbit
Channel Output Connector	2.4 mm
Interfaces	GPIB, LAN, parallel printer, VGA, 4 x USB 2.0, 1x USB 1.1

AUX In:
Lets you connect a signal to switch between Pattern A and B, or to suppress the output signal

Error Add:
Allows you connect an external trigger to insert a single bit error in the output

Trigger Out:
Lets you provide a trigger for another device

Sub Clock Out:
Provides a reference clock at subrates of the data rate.

Delay Control In:
Lets you use an external signal to control jitter in the data output.

Clock In:
Offers you to connect a clock signal from another device

Clock Out:
Frequency reference, can be set according to the logic family

Data Out:
Stimulus signal compatible with a wide variety of logic families and signals RZ, R1 ...

Keeping pace with technology and increasing speeds –
Are you ready for the next generation of applications?

The transfer of large amounts of data and spiraling transmission rates, needed for services such as video on demand and to ensure ever increasing Internet bandwidth, are driving speed increases in infrastructure and components. Signals break through one performance barrier after another. As electrical signals start competing with laser-generated ones, it is no longer necessary to convert to optical to reach high speeds.

High-speed protocols rely on a solid physical layer and dependable signal integrity. The next generations of protocols such as PCI Express, which in its second-generation doubles both clock rate and data throughput, raise the standards for jitter and sensitivity. Validation and

characterization become critical in ensuring effects such as reflection and crosstalk are kept within allowable limits.

As a developer you strive to keep pace with faster and more complex bus standards. Accelerated development cycles make proprietary test solutions less attractive. Instead you need standard instruments you can rely on to accomplish the job you need to get done. There can be no compromise on data quality, timing, synchronization and control.

**Table 2: Key requirements for physical layer testing (Addressed by 81141/2A)**

High-Speed Serial Buses			
PCI Express I, II	**S-ATA II, III**	**Fiber Channel**	**...**
Up to 5 GHz	**Up to 6 GHz**	**4 GHz**	
Low voltage differential signal		✓	
Receiver tests		✓	
• Jitter tolerance		✓	
• Receiver sensitivity		✓	
• Timing skew		✓	
• PLL loop bandwidth		✓	
500 MHz jitter modulation bandwidth		✓	
Sequencing for protocol data		✓	
Multiple pattern generation for protocol-like data		✓	
High-quality waveform for ultimate characterization		✓	

Applications in education and research e.g. control of particle accelerators	Ultra Wide Band Radio
Fast transition times	✓
Ultra-small pulses	✓
Trigger capabilities	✓

Agilents Offering of Leading Product Ranges

Agilent provides the most comprehensive portfolio of digital stimulus solutions to generate current and emerging digital waveforms and data signals. Agilent instruments cover a frequency range from 1mHz to 13 GHz, with pulse pattern and data generators and output amplitudes from 50 mV to 100 V.

The Agilent 81140A series serial Pulse Data Generator provides the smart way to measure – delivering the confidence you demand for your signal integrity in the next speed class.

- High-speed frequency up to 13 GHz
- High-quality waveforms with best transition times and lowest intrinsic jitter
- High flexibility data streams for stress test and application in education and research
    - Jitter insertion
    - Trigger capability
    - Sequencing and looping
    - Versatile pattern generation
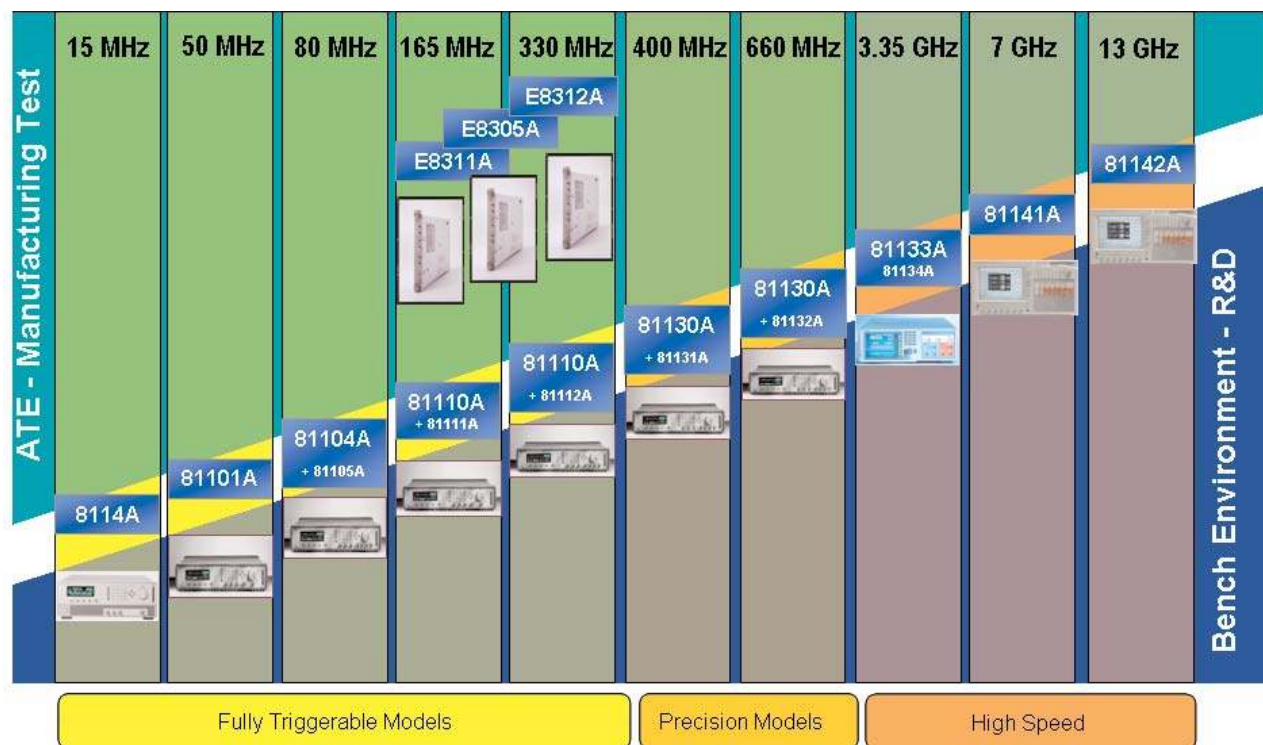
Versatile, highest quality pulse and data signal

High-speed and high-quality signals

Achieving high-quality character-ization and reliable measure-ments needs superior signal quality. As the frequency increases, accurate results rely on signal timing, transitions and integrity. With its outstanding rise and fall times and its matchless jitter performance the Agilent 81141/2A serial Pulse Data Generators are indispensa-ble extensions to even the most comprehensive instrument port-folio. The reliability of its test signal lets you focus on the measurement instead of the set up.

Picture 1: Precision low jitter RZ signal measured on a scope
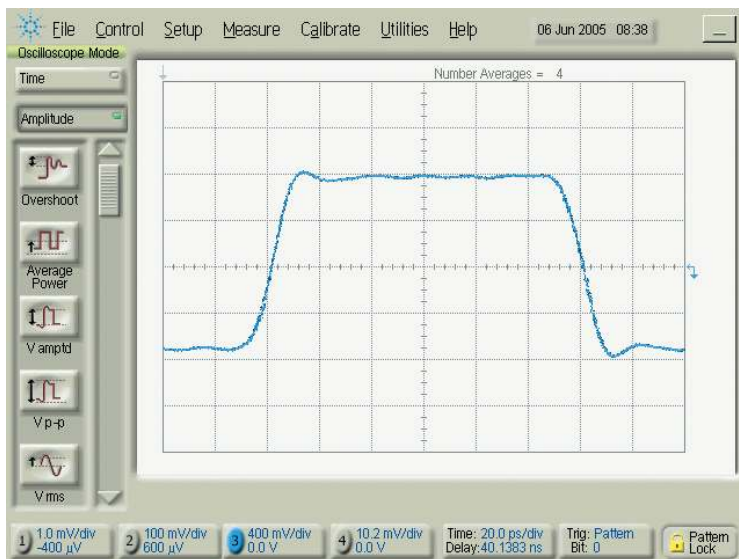
Data formats and flexible parameters

The variety of data formats available with the Agilent 81141/2A serial Pulse Data Generator supports a broad range of tests. Formats include R1 and NRZ, and RZ for band-width tests. Of course, parame-ters like width and duty cycle are configurable. You can even adjust cross points for your sensitivity tests.

Picture 2: Precision low jitter signal with cross-over
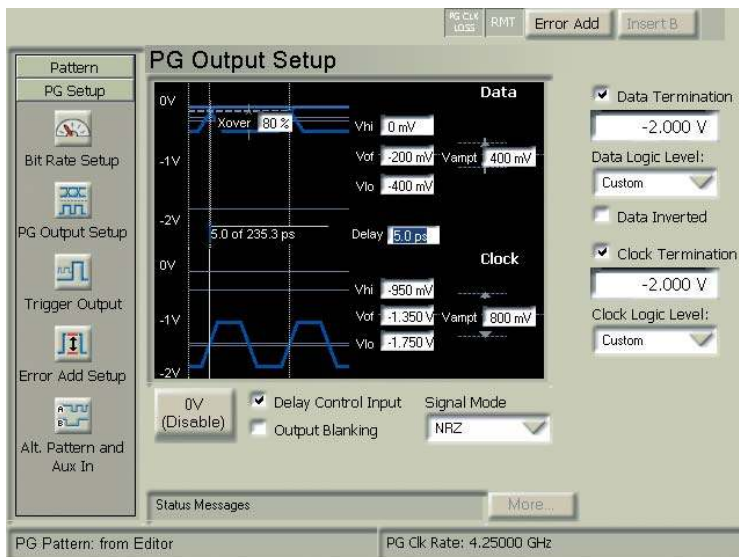
Full control of data streams for stress testing
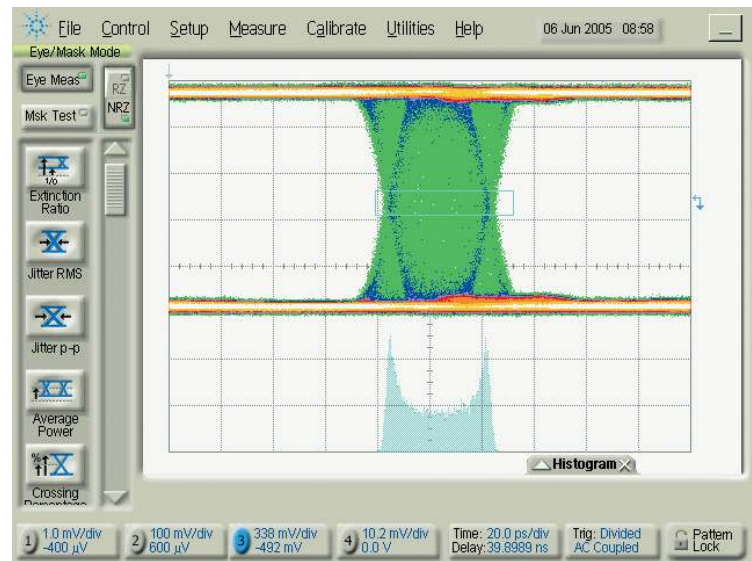
Jitter

Wide bandwidth insertion capability is essential for stressing your device to its limits. The external modulation input of the Agilent 81140A Series serial Pulse Data Generators let you control the extent and form of signal jitter, to emulate real world conditions. A variable crossover point provides further control for deteriorating the signal quality.

Delaying the data relative to the clock lets you generate high frequency, low amplitude jitter. Or you can apply an FM modulated clock to generate higher amounts of jitter at lower frequencies (wander).

Picture 4: Random jitter
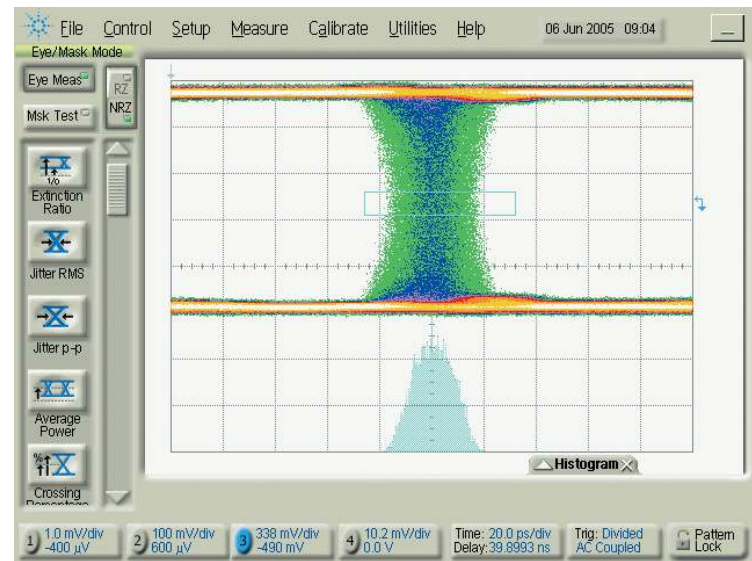
Picture 5: Sinusoidal jitter

Picture 3: Periodic Jitter: UI max vs. data rate (at modulation frequency: DC to 1 GHz)

Agilent 81141A 7 GHz serial Pulse Data Generator Data Sheet
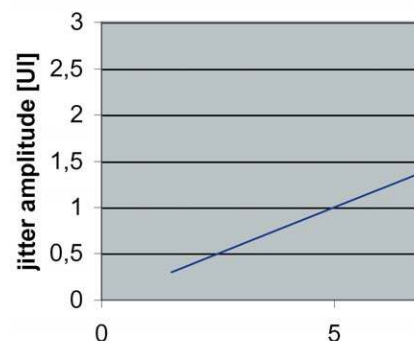
Pattern Generation

The Agilent 81141/2A serial Pulse Data Generator hardware is perfectly suited to long, high-speed random traffic (pseudo-random binary sequences) and memory-based patterns. These simulate the data your device might be subjected to in the real world. Multiple types of data pattern are available to present different data loads for your device. User-defined or software-generated patterns – representing any type of arbitrary data – can be loaded into memory. Software-generated patterns can be further modified with variable mark density to stress your device or system to its limit. The larger the pattern, the greater the stress. The pattern can also be repeated if, in case you require predictability for your debug. A collection of sample patterns for FDDI, Fiber Channel, SDH and SONET are available for the Agilent 81140A Series.

Sequencing and looping

Sequencing and looping of up to 4 blocks are available to address the needs for protocol emulation of S-ATA and PCI Express.
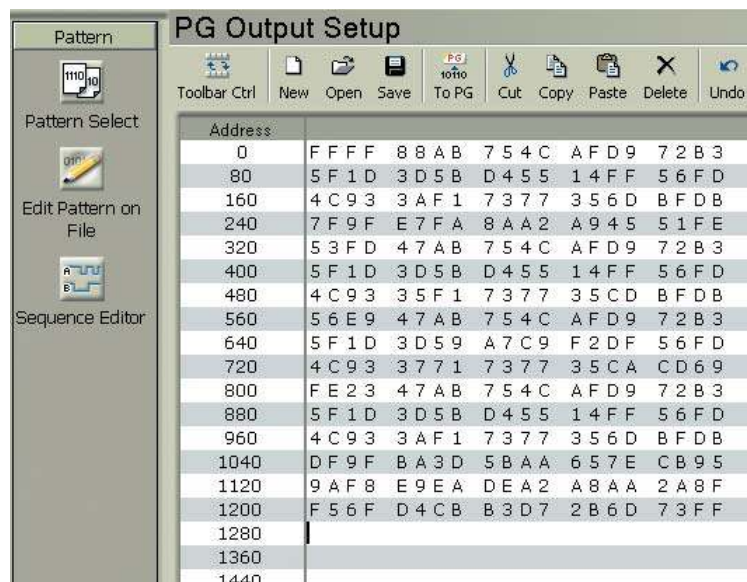
Trigger

Extensive triggering ensures the Agilent 81141/2A serial Pulse Data Generators can interact easily with other instruments.
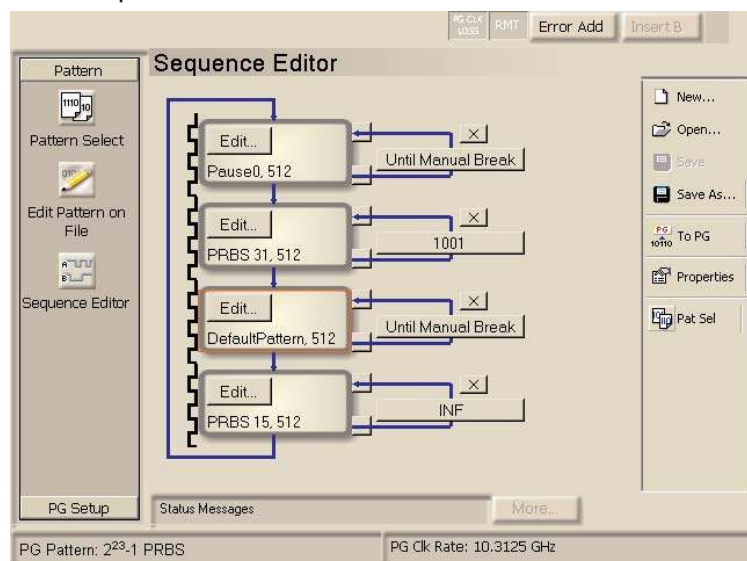There are two modes:
Trigger In (set up via Aux In) the Agilent 81141/2A serial Pulse Data Generators can select and run different pulses or data streams based on predefined signals or edges. This lets you define a trigger condition to start a data or pulse sequence, or, on the other hand, to suppress the output.
The Trigger Out of the Agilent 81141/2A serial Pulse Data Generator can send a trigger sequence for external devices, such as an oscilloscope.

Picture 6: Pattern Editor

Picture 7: Sequence Editor

Specifications

Data Output (DATA OUT)

Table 3: Specifications for Data Output

Range of operation	150 MHz to 7 GHz / 13.5 GHz
	For RZ/R1: min. 620 MHz; < 620 MHz only with external clock
	For RZ/R1/Pulse Up to 7GHz
Frequency accuracy	± 15 ppm typical
Width accuracy	± 20 ps
Format	NRZ, normal or inverted, RZ, R1
Amplitude/Resolution	0.10 V to 1.8 V, 5 mV step
Output voltage window	−2.0 V to +3.0 V
Predefined levels	ECL, PECL (3.3 V), LVDS, CML
Transition times	
(20 % to 80 %)	< 20 ps
(10 % to 90 %)	< 25 ps
Low Intrinisic Jitter	9 ps_{pp} typical
Clock/data delay range	±0.75 ns in 100 fs steps
External termination voltage	−2 V to +3 V
Crossing point	Adjustable from 20 % to 80 % typical
RZ/R1 width	70 ps to period −70ps
Pulse width	35 ps to period -35 ps (81142A only)
Single error inject	Adds single errors on demand
Fixed error inject	Fixed error ratios of 1 error in 10^n bits, n = 1...12
Interface	Differential or single-ended, DC coupled, 50 Ω
Connector	2.4 mm female

Clock Output (CLK OUT)

Table 4: Clock output characteristics.

Amplitude/Resolution	0.1 V_{pp} to 1.8 V_{pp}, 5 mV steps
Output voltage window	−2.00 V to +2.8 V
Transition times	
(20 % to 80 %)	< 20 ps
(10 % to 90 %)	< 25 ps
External termination voltage	−2 V to +3 V
Jitter	< 1 ps_{rms} typical
Interface	Differential or single-ended, DC coupled, 50 Ω output impedance
Connector	2.4 mm female

Subrate Clock Output (SUB CLK OUT)

The subrate clock output is used to generate reference clocks that are subrates of the data rate, e.g. the 100 MHz clock for PCI Express (2.5 GHz data rate).

Table 5: Specifications for Subrate Clock Output

Divider factors	N = 2, 3 ... 128
Levels	High: +0.5 V
	Low: −0.5 V typical
Transition times	35 ps typical
Interface	DC coupled, 50 Ω
Connector	SMA female

Clock Input (CLK IN)

Uses an external clock as generator clock.

Table 6: Specifications for Clock Input

Amplitude	200 mV to 2 V
Interface	AC coupled, 50 Ω nominal
Connectors	SMA female, front panel

10 MHz Reference Input (10 MHZ REF IN)

If a 10 MHz reference clock is applied, the PLL generating the internal clock for the generator will lock to the applied signal.

Table 7: Specifications 10 MHz Reference Input

Amplitude	200 mV to 2 V
Interface	AC coupled, 50 Ω nominal
Connectors	BNC, rear panel.

10 MHz Reference Output (10 MHZ REF OUT)

Uses an external clock as generator clock.

Table 8: Specifications 10 MHz Reference Output

Amplitude	1 V into 50 Ω typical
Interface	AC coupled, 50 Ω output impedance
Connectors	BNC, rear panel

Delay Control Input (DELAY CTRL IN)

The external signal applied to Delay Control Input, varies the delay between Data Output and Clock Output. This can be used to generate jittered signals to stress the device under test.

Table 9: Specifications for Delay Control Input

Range	−100 ps to +100 ps
Sensitivity	400 ps/V typical
Linearity	±5 % typical
3dB modulation bandwidth	DC to 1 GHz
Levels	−250 mV to +250 mV
Interface	DC coupled, 50 Ω nominal
Connector	SMA female

Error Add Input (ERROR ADD)

The Error Add input adds a single error to the data output for each rising edge at the input.

Table 10: Specifications for Error Add Input

Levels	TTL compatible
Interface	DC coupled, 50 Ω nominal
Connector	SMA female

Trigger Output (TRIGGER OUT)

This provides a trigger signal synchronized with the pattern, for use with an oscilloscope or other test equipment. There is a delay of 32 ns typically between trigger and data output for data rates ≥ 620 MHz. The two modes are pattern trigger and divided clock trigger.

Pattern Trigger Mode: for PRBS patterns, the pulse is synchronized with a user specified trigger pattern. One pulse is generated for every 4th PRBS pattern.

Divided Clock Mode: the trigger is a square wave at the clock rate divided by 2, 4, 8, 10, 16, 20, 32, 64, and 128.

Table 11: Specifications for Trigger Output

Pulse width	Square wave
Transition times	35 ps typical
Levels	High: +0.5 V; Low −0.5 V typ.
Interface	DC coupled, 50 Ω nominal, single ended or differential
Connector	SMA female

AUX Input (AUX IN) (Trigger In)

When the Alternative Pattern Mode is activated, the memory will be split into two parts. The user can define a pattern for each part. Depending on the operational mode of the Auxiliary Input, the user can switch the active pattern in real-time by applying a pulse (Mode 1) or a logical state (Mode 2) to the Auxiliary Input. If the Alternative Pattern Mode is not activated, the user can suppress the data on the data output by applying a logical high to the Auxiliary Input (Mode 3).

Table 12: Specifications for Auxiliary Input

Levels	TTL compatible
Interface	DC coupled, 50 Ω nominal
Connector	SMA female

Pattern

PRBS
$2^n - 1$ and 2^n with $n = 7, 10, 11, 15, 23, 31$
User-definable pattern: 32 Mbit, independent for pattern generator and error detector.

Sequencing
Pattern sequences can be started by command or by a signal at Aux Input.
Number of blocks: up to 4. The block resolution of user definable pattern is 512 bit.
Loops: over 4 or fewer blocks.

Alternative Pattern
Switch between two equal length user programmable patterns, each up to 16,777,216 bits (16 Mbit). Switching is possible using a front panel key or the auxiliary input port, or over GPIB. Changeover is synchronous with the end of the pattern. The length of the alternating patterns should be a multiple of 512 bits. Two methods of controlling pattern changeover are available: one-shot and alternative.

Zero Substitution
Zeros can be substituted for data to extend the longest run of zeros in any of the library of predefined patterns. The longest run can be extended to the pattern length − 1. The bit following the substituted zeros is set to 1.

Variable Mark Density
The ratio of ones to total bits in any of the library of predefined patterns can be set to 1/8, 1/4, 1/2, 3/4, or 7/8.

Library of predefined patterns:
SONET, SDH, FDDI, Fiber Channel.

Table 23: General Characteristics

Operating temperature	5 °C to 40 °C
Storage temperature	−40 °C to +70 °C
Operating Humidity	5 °C to 40 °C, 95 % relative humidity, non-condensing
Storage Humidity	>50 °C to 70 °C, 50% relative humidity
Power requirements	100 VA to 240 VA, ±10 %, 47 Hz to 63 Hz, 350 VA
Physical dimensions	Width: 424.5 mm
	Height: 221.5 mm
	Depth: 580.0 mm
Weight (Net)	24.5 kg
Weight (shipping) (Max)	36.0 kg
Recommended recalibration period	1 year
Warranty period	1 year. Extended warranty available.

Display
8" color LCD touch screen
Data Entry
• Color touch screen display, numeric keypad with up/down arrows, dial-knob control or external keyboard and mouse via USB interface
• Pattern Export/Import
Hard Disk
For local storage of user patterns and data. An external disk is also available for connection via USB interface.
Interfaces
GPIB (IEEE 488), LAN, parallel printer port, VGA output, 4 x USB 2.0, 1 x USB 1.1 ports
Operating System
Microsoft Windows XP
Regulatory Standards
Safety:IEC 61010-1:2001, EN 61010-1:2001 CAN/CSA-C22.2 No.61010-1-04
UL 61010-1:2004
EMC: EN 61326:1997 + A1:1998+A2:2001, IEC 61326:1997+A1:1998+A2:2000
Quality Management: ISO 9004
Specification Range of Validity
The specifications in this brochure describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid in a range from 5°C to 40°C ambient temperature after 30 minutes warm-up phase. All measurements are carried out at ECL Level. If not otherwise stated, all inputs and outputs need to be terminated with 50 Ohms to ground. All specifications, if not otherwise stated, are valid using the recommended cable set N4910A (2.4 mm, 24" matched pair).

Agilent's IO libraries Suite ships with the 81140 series to help you quickly establish an error-free connection between your PC and instruments-regardless of the vendor. It provides robust instrument control and works with the software development environment you choose.

Related Literature	Publication Number
Pulse Pattern Family Brochure	5980-0489E

Ordering Instructions

7 GHz serial Pulse Data Generator	**81141A /**
13 GHz serial Pulse Data Generator	**81142A**

4x 50 Ω, terminations,
4 2.4mm male to female adaptor 50 W SMA termination.
1 Stylus Palm Touchscreen pen

Warranty:	
Extended Warranty	**R1280A**
Calibration:	**R1282A**
Commercial Calibration	
with test data	**81141A-UK6 /**
	81142A-UK6
Recommended Accessories:	
2.4 mm cable kit	**N4910A**

Complementary Products:
Agilent Oscilloscopes
(Real-time or Sampling) DSO80000/DA-J

The new Agilent INfiniium 80000 Series oscillloscopes and Agilent InfiniiMax II Series probes are the highest signal integrity measurement system available.
• Up to 13 Ghz bandwidth and 40 GSa/s sample rate to the probe tip
• Lowest trigger jitter in the industry
• Unrivaled InfiniiMax II probe heads support solder-in, browsing, socket and SMA use models up to 13 GHz bandwidth. This i sthe only probe systemin the market to offer this level of performance and usability.

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⊙ **Agilent Open**

Agilent Open simplifies the process of connecting and programming test systems to help engineers design, validate and manufacture electronic products. Agilent offers open connectivity for a broad range of system-ready instruments, open industry software, PC-standard I/O and global support, which are combined to more easily integrate test system development.

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